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| UNIVERSITY OF INFORMATION TECHNOLOGY  **COMPUTER ENGINEERING DEPARTMENT** | **FINAL EXAMINATION II (2018-2019)**  **COURSE: DEGITAL LOGIC DESIGN**  *Time duration: 90 minutes*  *(Paper materials are allowed)* |

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| **STUDENT NAME: ……………………………………ID: …………..ORDER:…** |

# Question 1 (3 points)

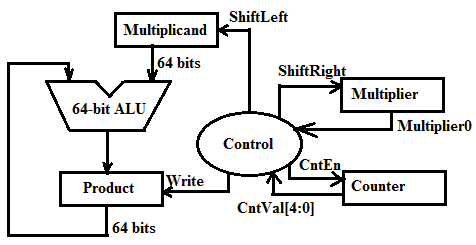
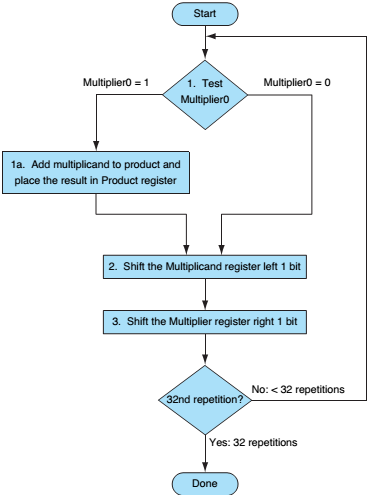


Figure 1: Multiplication circuit

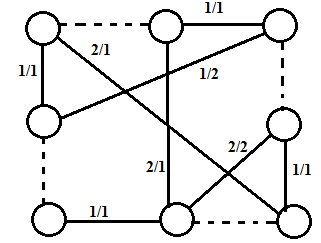
Based on Multiplication circuit and its ASM on

Figure 1 and Figure 2, please derive the Moore-

FSM to design the Control module for Multiplication

circuit. Figure 1: Multiplication ASM

# Question 2 (3 points)

Group the nodes specified by the compatibility graphs

showed in Figure 3.

Figure 3: Compatibility graph



# Question 3 (4 points)

Construct a pipelined data-path for the Square-Root Approximation (SRA) circuit by dividing an SRA algorithm into three stages as Figure 4. Then, derive its timing diagram.

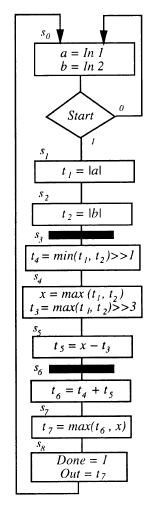


Figure 4: ASM for three-stages SRA





**This examination’s learning outcomes (LO) (matching to subject syllabus’s LO)**

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| **Question** | **LO** | **Description** |
| 1 | G1 | **Be able to design the controller** |
| 2 | G2 | **Be able to optimize the design** |
| 3 | G3 | **Be able to design and analyze digital circuit** |

**Approved by Head of Subject Designed by**

**Lâm Đức Khải Lâm Đức Khải**